1 (Sem–4/FYUGP) PHY 43 MJ

2026

PHYSICS

(Major)

Paper : PHY4400304MJ

(Analog Electronics)

Full Marks : 45

Time : 2 hours

The figures in the margin indicate full marks for the questions.

1. Answer the following questions : 1×5=5

(a) In a PN junction, the region containing uncompensated acceptor and donor ions is called the :

(A) Neutral region

(B) Depletion region

(C) Active region

(D) Diffusion region

(Choose the correct option)

(b) State whether the following statement is True ***or*** False :

"Applying negative feedback to an amplifier increases its voltage gain while improving its stability."

(c) Name the primary condition for self-sustained oscillations in an amplifier circuit.

(d) The _____ is the maximum rate of change of output voltage per unit time in case of Op-Amp.

(Fill-up the blank)

(e) In CRO, what type of waveform is generated by the time base circuit to move the electron beam horizontally ?

2. Answer the following questions : ***(any five)*** 2×5=10

(a) Calculate the drift velocity of electrons in a semiconductor if the electron mobility is $1350 cm^2/V.s$ and the applied electric field is $100 V/cm$.

(b) Draw the circuit diagram of a voltage regulator using Zener diode.

(c) Mention *two* differences between *fixed bias* and *voltage divider bias* for transistor amplifiers.

(d) A transistor has a common-base current gain (α) of 0.98. Calculate its common-emitter current gain (β).

(e) What do you mean by the *active region* for a transistor amplifier ?

(f) Why is a coupling capacitor used between the two stages of an RC-coupled amplifier ?

(g) An amplifier has an open-loop voltage gain (A) of 1000. If negative feedback with a feedback fraction (β) of 0.04 is applied, calculate the gain with feedback (A_f).

(h) Calculate the frequency of oscillation for an RC Phase Shift Oscillator if $R = 10k\Omega$ and $C = 0.01\mu F$.

(i) Draw the basic circuit diagram for an inverting amplifier and write the formula for its closed-loop voltage gain.

(j) Write *two* differences between Class *B* and Class *C* amplifiers.

3. Answer the following questions : ***(any four)*** 5×4=20

(a) (i) Explain the concept of "Virtual Ground" in an Op-Amp. Why is it significant for circuit analysis ? 2+1=3

(ii) For a closed loop non-inverting amplifier, the resistors are $R_f = 47k\Omega$ and $R_1 = 4.7k\Omega$. If the output voltage is measured at $11V$, what was the applied input voltage ? 2

(b) (i) Explain the "Summing Amplifier" configuration in inverting mode. 2

(ii) A summing amplifier has three input resistors : $R_1 = 10k\Omega$, $R_2 = 20k\Omega$, and $R_3 = 50k\Omega$. The feedback resistor is $R_f = 100k\Omega$. If $V_1 = 1V$, $V_2 = -2V$ and $V_3 = 3V$, find the output voltage. 3

(c) (i) What is the purpose of the Time Base Generator in a CRO ? What happens to the display if the time base is turned off ? 2

(ii) The horizontal "Time/Div" control is set to $2ms/div$. One complete cycle of a signal occupies 2.5 horizontal divisions. Calculate the period (T) and the frequency (f) of the signal. 3

(d) Explain how a CRO is used for the measurement of Phase difference using Lissajous Pattern.

(e) Draw the circuit diagram of a RC Phase shift oscillator. Derive the expression for its frequency of Oscillation.

(f) Explain how negative feedback improves the "Gain Stability" of an amplifier.

(g) A negative feedback of $B = 0.002$ is applied to an amplifier of gain 1000. Calculate the percentage of change in overall gain of the feedback amplifier if the internal amplifier is subjected to gain reduction of 15%.

(h) In an RC coupled amplifier, the coupling capacitor C_C is $0.1\mu F$ and the input resistance of the second stage R_{in2} is $2k\Omega$. The output resistance of the first stage R_{o2} is $10k\Omega$.

(a) Calculate the lower (3-dB) cutoff frequency (f_L) of the coupling network.

(b) If the frequency of the input signal is reduced to $50Hz$, explain qualitatively what happens to the voltage gain.

3+2=5

4. Answer the following questions : ***(any one)*** 10

(a) (i) Define a step junction and explain the distribution of charge carriers across its depletion region.

1+2=3

(ii) Deduce an expression for barrier width of a PN junction. 7

(b) (i) Draw the circuit diagram of a Full-wave Bridge Rectifier and explain its working during both positive and negative half-cycles of the AC input. 2+3=5

(ii) A bridge rectifier uses four identical diodes, each having a forward resistance r_f of $10k\Omega$. The secondary voltage of the transformer is $20V$ (rms) and the load resistance (R_L) is 400Ω. Calculate the DC output voltage and the Rectification Efficiency. 5

(c) (i) Explain the concept of DC Load Line in transistor characteristics. How is it used to find the Q-point? 2+1=3

(ii) Explain the "Load Line" shift that occurs if the load resistance is changed while the supply voltage remains constant. 2

(iii) Find the collector current (I_C) and collector-emitter voltage (V_{CE}) for a circuit where $V_{CC} = 12V$, $R_C = 2k\Omega$, and the transistor is at cutoff. 2+3=5

(d) (i) Represent a transistor as a 2-port network and define the four h-parameters (h_{ie}, h_{re}, h_{fe}, h_{oe}) for a Common Emitter configuration. 3

(ii) Draw the h-parameter equivalent circuit of a single-stage CE amplifier. 2

(iii) For a CE amplifier, the h-parameters are $h_{ie} = 1.1k\Omega$, $h_{fe} = 50$, $h_{re} = 2.5 \times 10^{-4}$ and $h_{oe} = 25\mu A/V$. If the load resistance (R_L) is $2k\Omega$, calculate the Current Gain and Input Impedance. 5